CLAIMS:

What is claimed is:

1. A traffic management processor for scheduling packets for transmission across a network, comprising:

a departure time calculator for generating a departure time for each packet;

a departure time table having a plurality of rows, each having a first portion for storing the departure time for a corresponding packet and having a second portion for storing a rollover bit; and

a reset circuit coupled to the departure time calculator and to the departure time table, the reset circuit configured to reset the rollover bits from a first logic state to a second logic state at a predetermined time.

2. The traffic management processor of Claim 1, wherein the departure time calculator comprises:

a counter for generating an arrival time; and

an arithmetic logic unit coupled to the counter and configured to generate the departure in response to the arrival time.

3. The traffic management processor of Claim 2, wherein the reset circuit has an output to provide a reset signal to the departure time table, wherein the reset signal is asserted to reset the rollover bits when the counter reaches a value indicative of the predetermined time.

4. The traffic management processor of Claim 1, further comprising:

compare logic coupled to the departure time table and configured to compare the departure times with each other to

determine which departure time is the earliest.

5. The traffic management processor of Claim 1, wherein each rollover bit comprises a most significant bit of the corresponding departure time.

6. A traffic management processor for scheduling packets for transmission across a network, comprising:

a counter for generating an arrival time for each packet;

an arithmetic logic unit having an input to receive the arrival time and configured to generate a departure time in response to the arrival time;

a reset circuit having an input to receive the arrival time and having an output for generating a reset signal; and

a table for storing having a plurality of rows, each having a first portion for storing the departure time for a corresponding packet and having a second portion for storing a rollover bit, wherein the reset signal selectively resets the rollover bit from a first logic state to a second logic state in response to the reset signal.

7. The traffic management processor of Claim 6, wherein the reset circuit asserts the reset signal to reset the rollover bits when the counter generates a maximum arrival time.

8. The traffic management processor of Claim 6, wherein each rollover bit comprises a most significant bit of the corresponding departure time.

9. The traffic management processor of Claim 6, further comprising:

compare logic coupled to the table and configured to

compare the departure times with each other to determine which departure time is the earliest.

10. A method for operating a packet scheduler, comprising:

determining an arrival time for each packet received;

calculating a departure time each packet in response to the packet's arrival time;

storing the departure times in a departure time table;

asserting a rollover bit corresponding to each departure time; and

de-asserting the rollover bits when the arrival time reaches a maximum value.

11. The method of Claim 10, wherein the de-asserting comprises:

comparing the arrival time with the maximum value; and

selectively asserting a reset signal in response to the comparing.

12. The method of Claim 11, further comprising:

resetting the rollover bits to a logic low value in response to the reset signal.